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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER |
|---|
| NGUYEN, DONGHAI D |

| ART UNIT | PAPER NUMBER |
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| 3729 | 2 |

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DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/091,743 | Applicant(s) THOMAS ET AL. | |
|---|---|---|---|
| | Examiner Donghai D. Nguyen | Art Unit 3729 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *23-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-30* are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-22, drawn to an integrated circuit and method for fabricating thereof, classified in class 29, subclass 841.

   II. Claims 23-30, drawn to method for fabricating an integrated circuit, classified in class 29, subclass 825.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require the passivation layer or via of the subcombination. The subcombination has separate utility such as chip carrier.

3. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with William Esser on March 18, 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1022. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Specification*

7. The abstract of the disclosure is objected to because the claimed invention is an integrated circuit and a method of making an integrated circuit. Correction is required. See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 3-9, 13-18, and 21-22, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 3 and 13, it is unclear as to what happen to a vertical plug mounted to the metal pad when layers of undoped silicon oxide, phosphosilicate glass, and silicon oxynitride disposed on the active circuit area and on the metal pad. Furthermore how the redistribution metal layer electrically connected to the vertical plug, if it covers by the layers.

Regarding claims 5 and 15, it is uncertain how the redistribution metal layer electrically connected to the metal pad when the undoped silicon oxide, phosphosilicate glass, and silicon oxynitride layers is covered/disposed on the metal pad.

Regarding to claims 7 and 17, it is unclear how a silicon oxynitride layer is deposited over all portions of said redistribution metal layer when another silicon oxynitride layer already deposited over all portions of said redistribution metal layer in the last step of claims 5 and 15.

### *Claim Rejections - 35 USC § 102*

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) The invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

11. Claims 1, 2, 10-12, 19-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art.

Applicant Admitted Prior Art's Fig. 1, discloses an integrated circuit and a method for fabricating an integrated circuit comprising the steps of: fabricating a portion of an integrated circuit (100) comprising at least one active circuit area (170); and fabricating a redistribution metal layer (140) in said integrated circuit during a fabrication process of said portion of said

integrated circuit; fabricating portions of said redistribution metal layer that are open to receive a solder bump (120), which attached to said portions of said redistribution metal layer; and said redistribution metal layer using a last metal layer that is used to fabricate an active circuit area of said integrated circuit.

> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-3, 5-8, 10-13, 15-17, 19-20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,441,467 to Toyosawa et al.

Regarding claims 1 and 10, Toyosawa et al disclose an integrated circuit and a method for fabricating an integrated circuit comprising the steps of: fabricating a portion of an integrated circuit comprising at least one active circuit area (20); and fabricating a redistribution metal layer (14) in said integrated circuit during a fabrication process of said portion of said integrated circuit;

Regarding claims 2, 6, 12, 20, and 22, Fig. 1 shows portion of said redistribution metal layer that are open to receive a solder bump (30).

Regarding claims 3 and 13, Toyosawa et al disclose the steps of: fabricating an active circuit area (3) and an associated metal pad (9a, b) on a base substrate (1); fabricating a vertical plug (vertical portion of part 14) of a redistribution metal layer (14); mounting said vertical plug of said redistribution metal layer on said metal pad (Fig. 4f); electrically connecting said vertical plug of said redistribution metal layer to said metal pad (Fig. 4f); depositing an undoped silicon oxide layer (10a) on said active circuit area and on said metal pad; depositing a phosphosilicate

glass layer (10b) on said undoped silicon oxide layer; depositing a silicon oxynitride layer (10c) over said phosphosilicate glass layer; depositing a flat redistribution metal layer (14) over said silicon oxynitride layer; and electrically connecting said flat redistribution metal layer to said vertical plug of said redistribution metal layer (Fig. 4f).

Regarding claims 5, 7-8, and 15-17, Toyosawa et al disclose the steps of: fabricating an active circuit area (3) and an associated metal pad (9a,b) on a base substrate (1); depositing an undoped silicon oxide layer (10a) on said active circuit area and on said metal pad; depositing a phosphosilicate glass layer (10b) on said undoped silicon oxide layer; depositing a redistribution metal layer (14) over said phosphosilicate glass layer; electrically connecting said redistribution metal layer to said metal pad; and depositing a silicon oxynitride layer (15) over portions of said redistribution metal layer (fig. 13 b).

Regarding claim 10 and 19, Figs. 4f and 13b show the redistribution metal layer using a last metal layer that is used to fabricate an active circuit area of said integrated circuit.

### *Allowable Subject Matter*

13. Claims 4, 9, 14, 18, and 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

### *Conclusion*

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (703) 305-7859. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (703) 308-1789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN

PETER VO
SUPERVISORY PATENT EXAMINER
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